FIG. 1

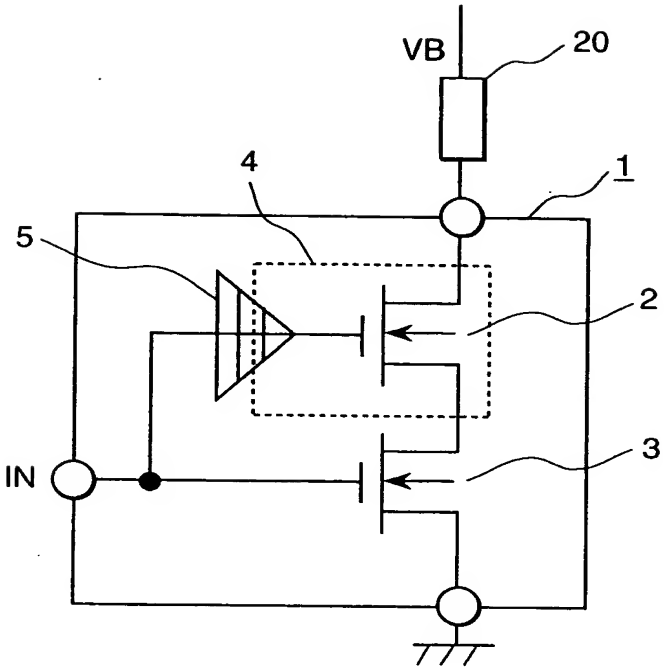


FIG. 2

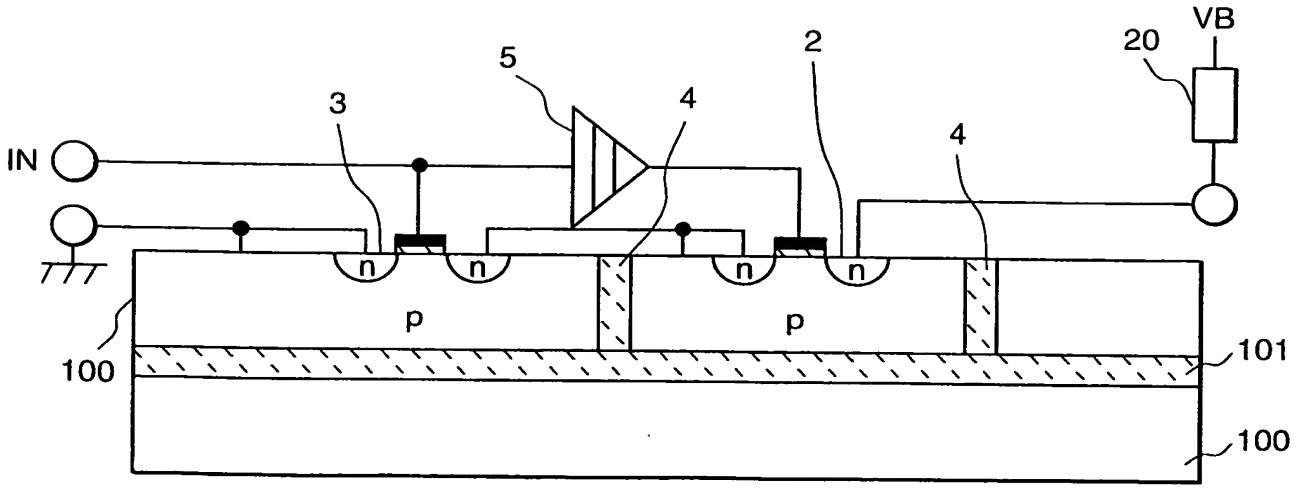


FIG. 3

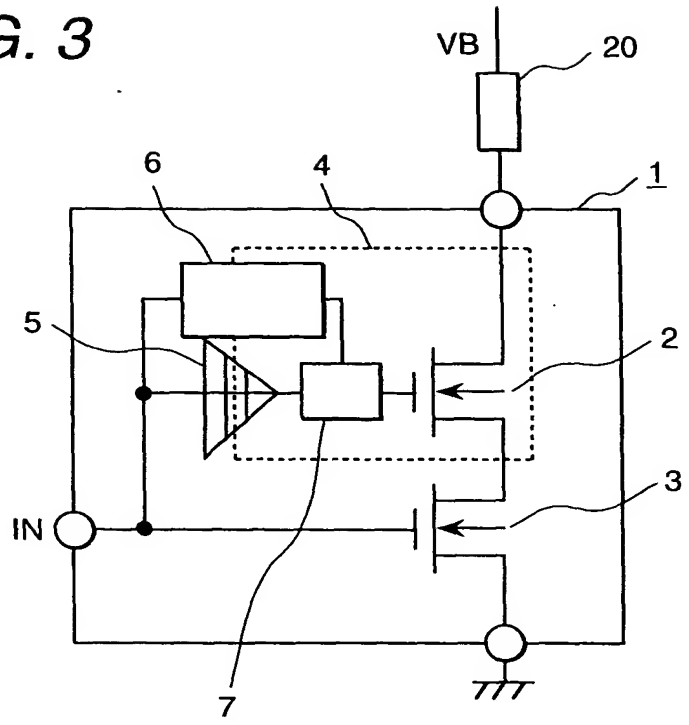


FIG. 4

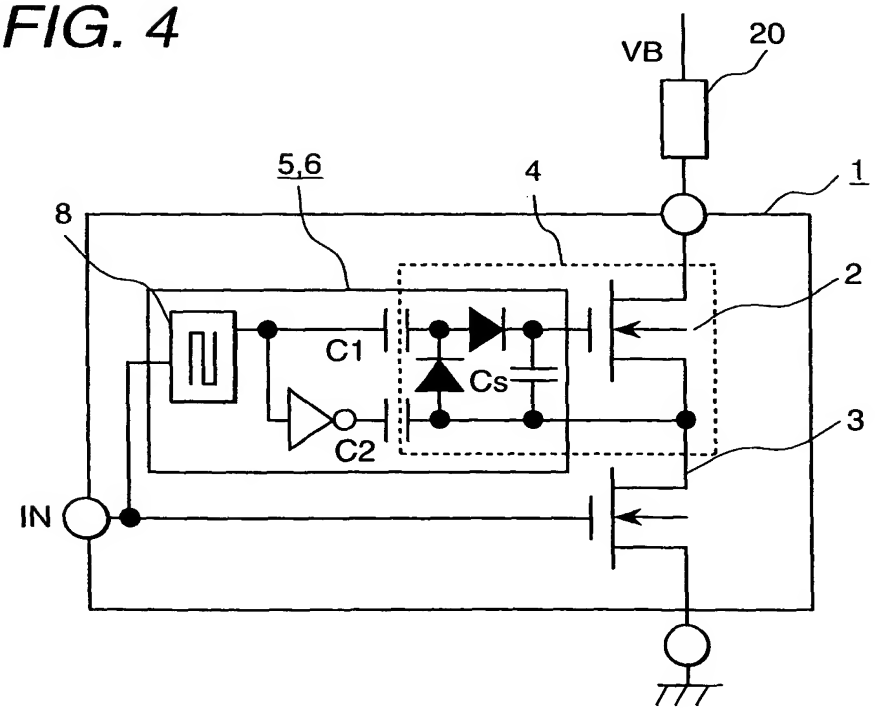


FIG. 5

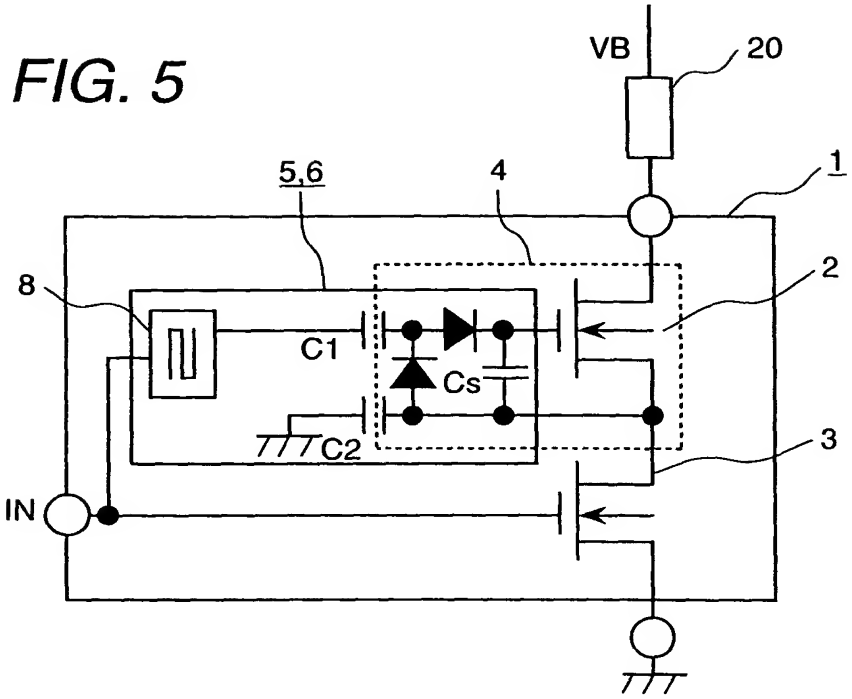


FIG. 6

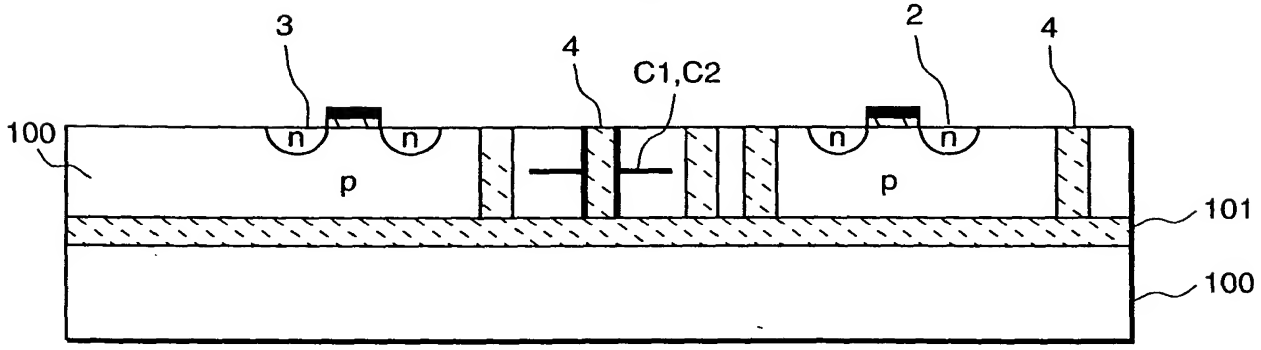


FIG. 7

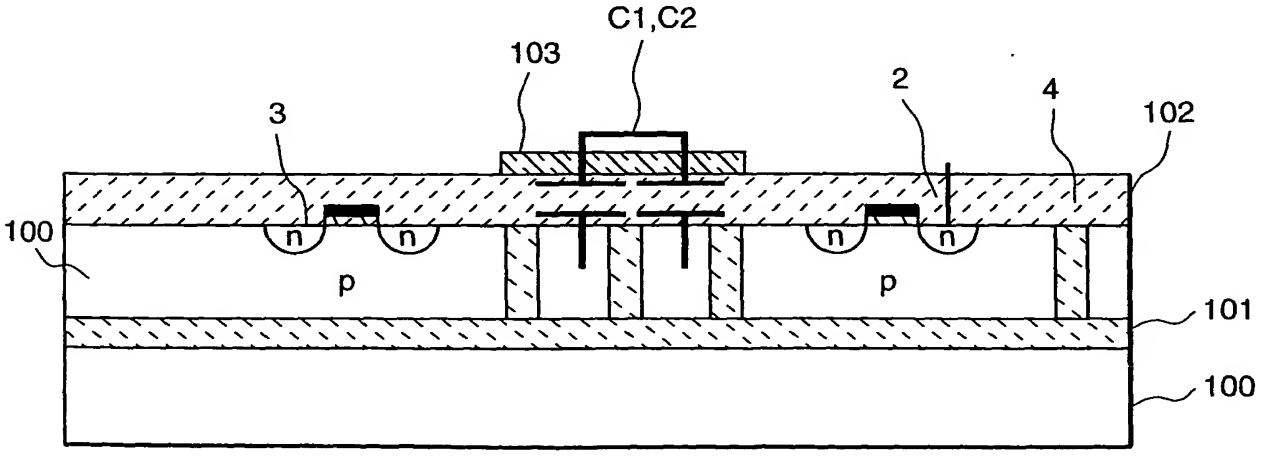


FIG. 8

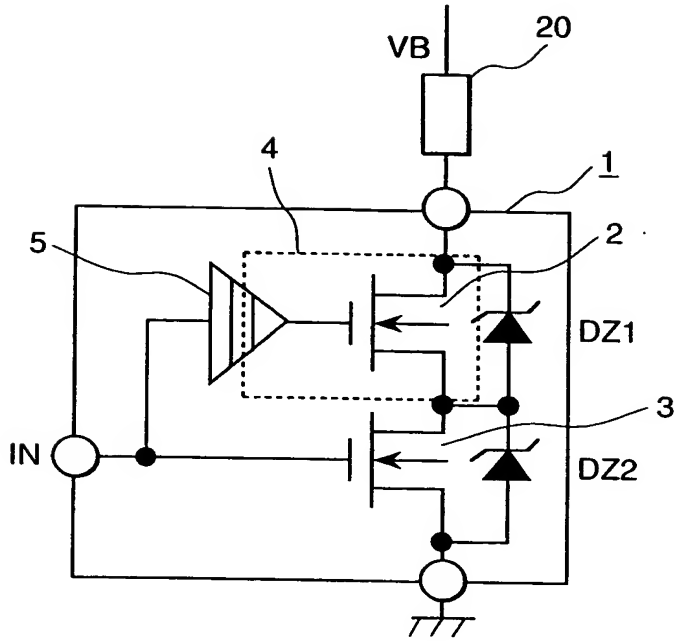


FIG. 9

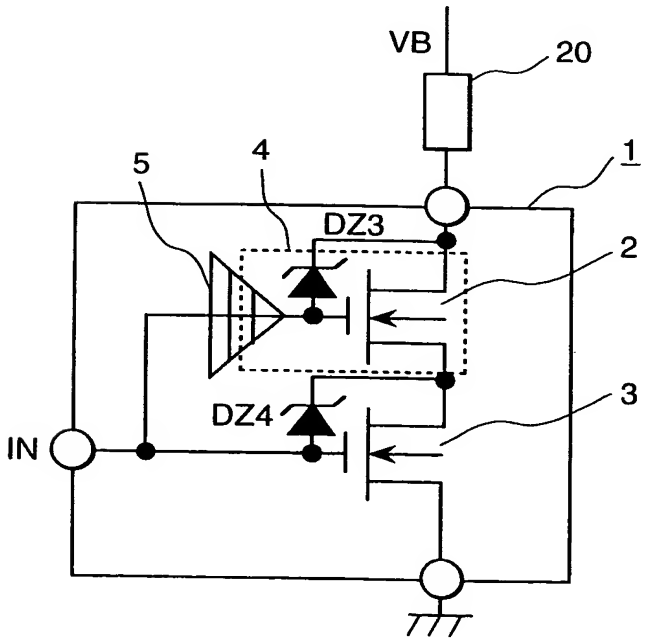


FIG. 10

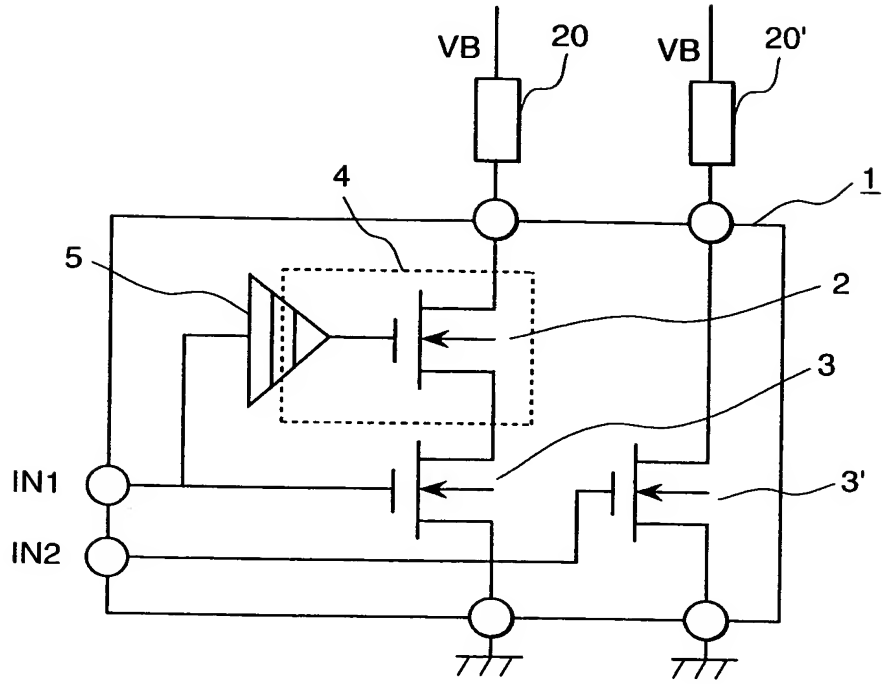


FIG. 11

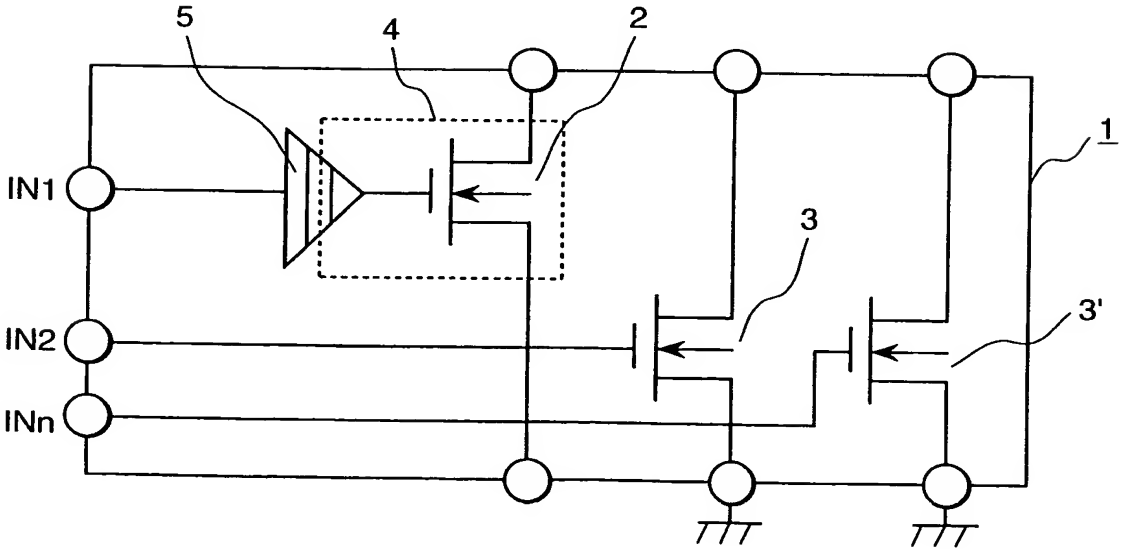


FIG. 12

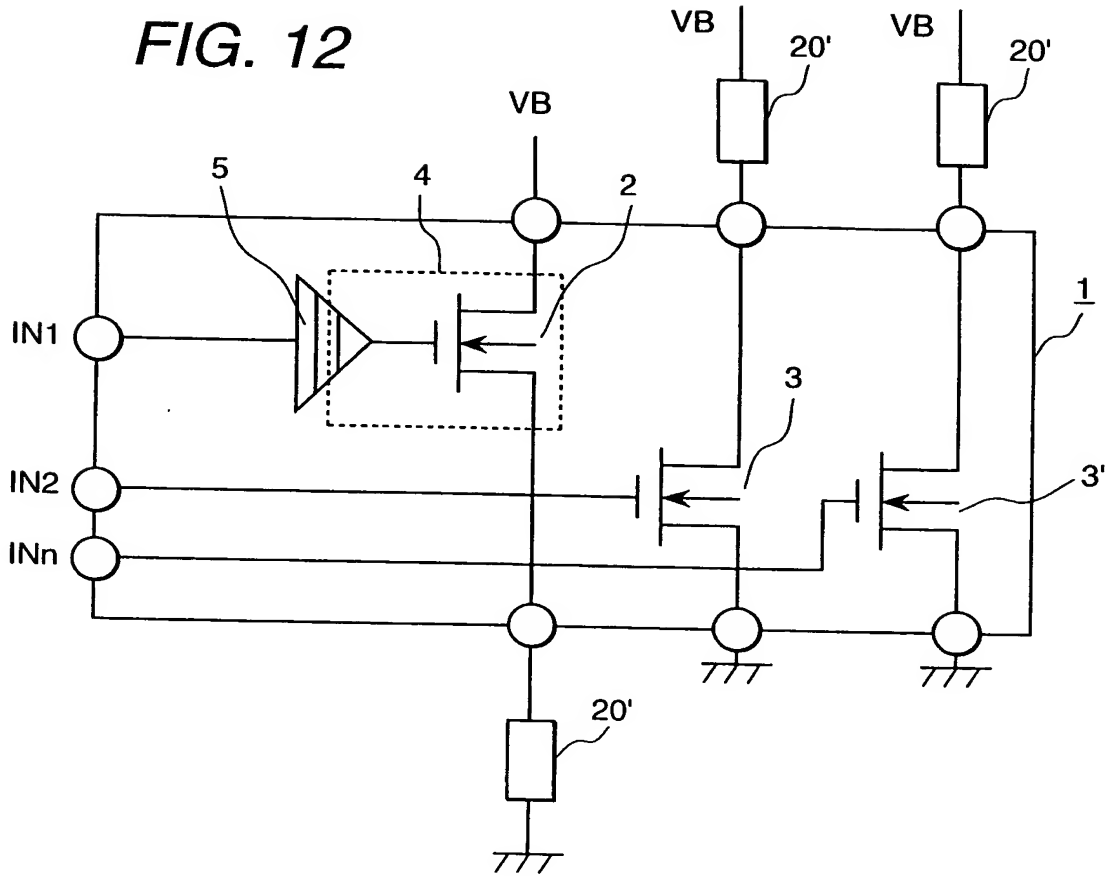

VB
20'
VB
20'
VB
5
4
2
1
IN1
3
IN2
3'
INn
20'

FIG. 13

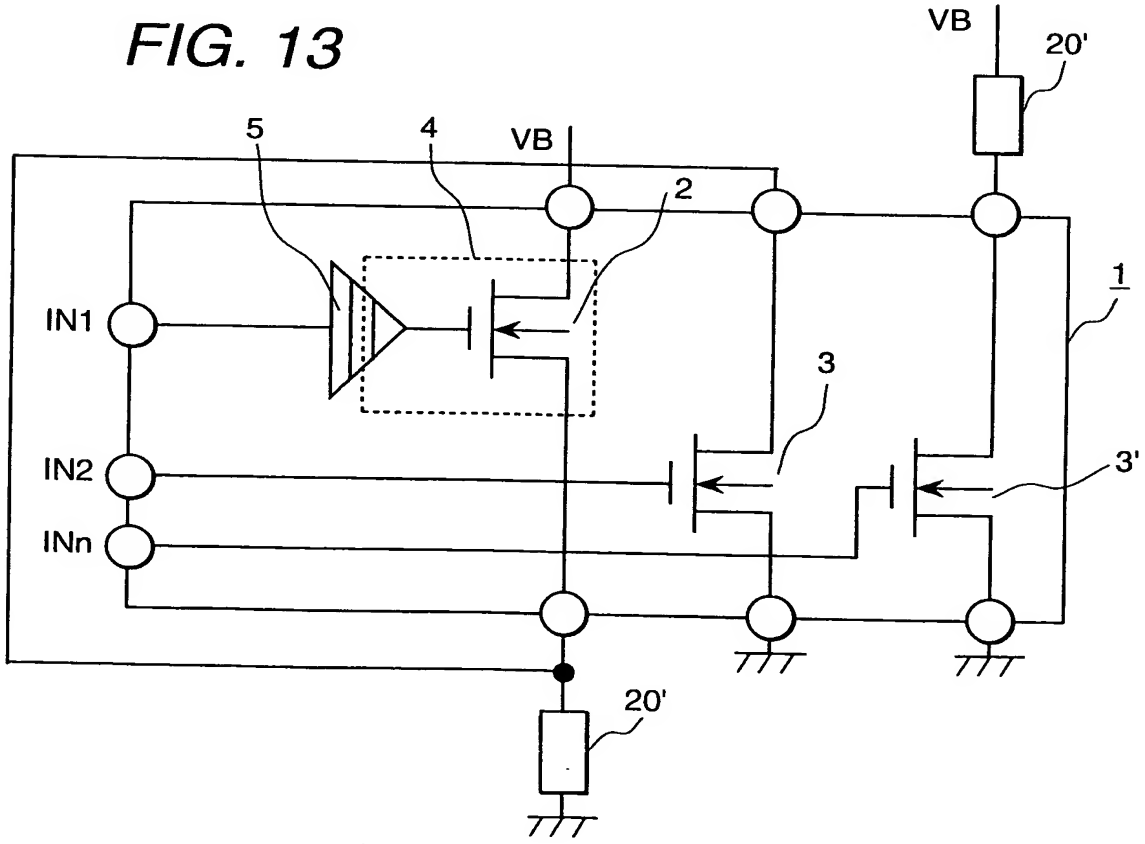

VB
20'
5
4
VB
2
1
IN1
3
IN2
3'
INn
20'

FIG. 14

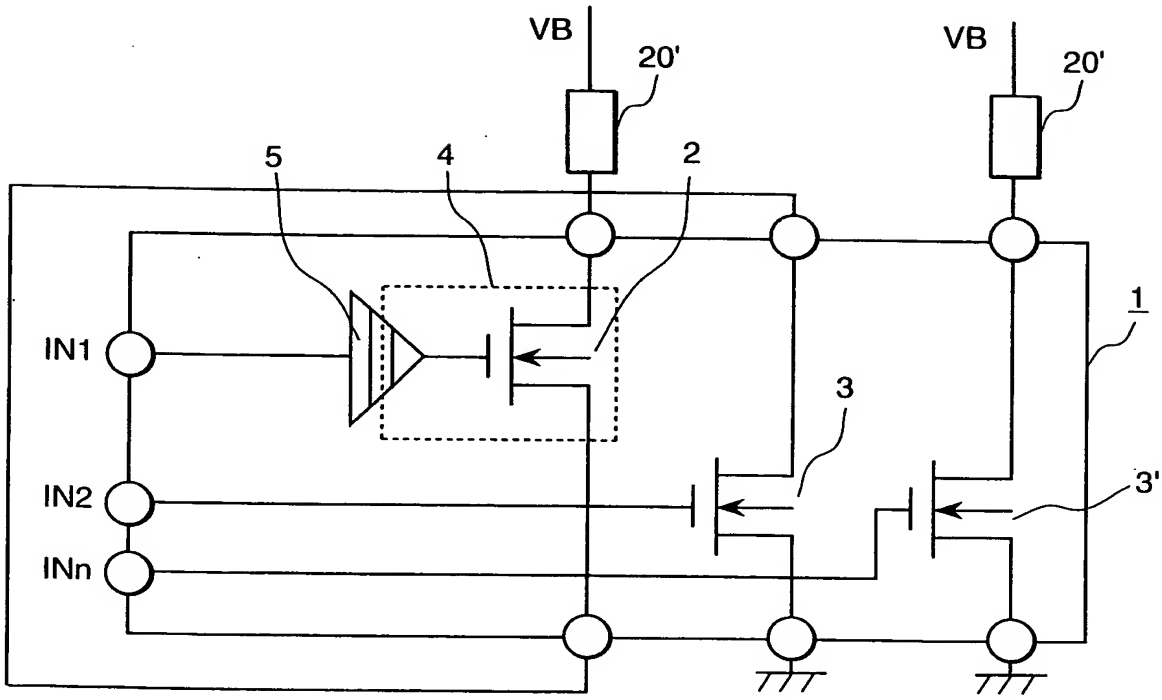

VB
20'
VB
20'
5
4
2
1
IN1
3
IN2
3'
INn

FIG. 15

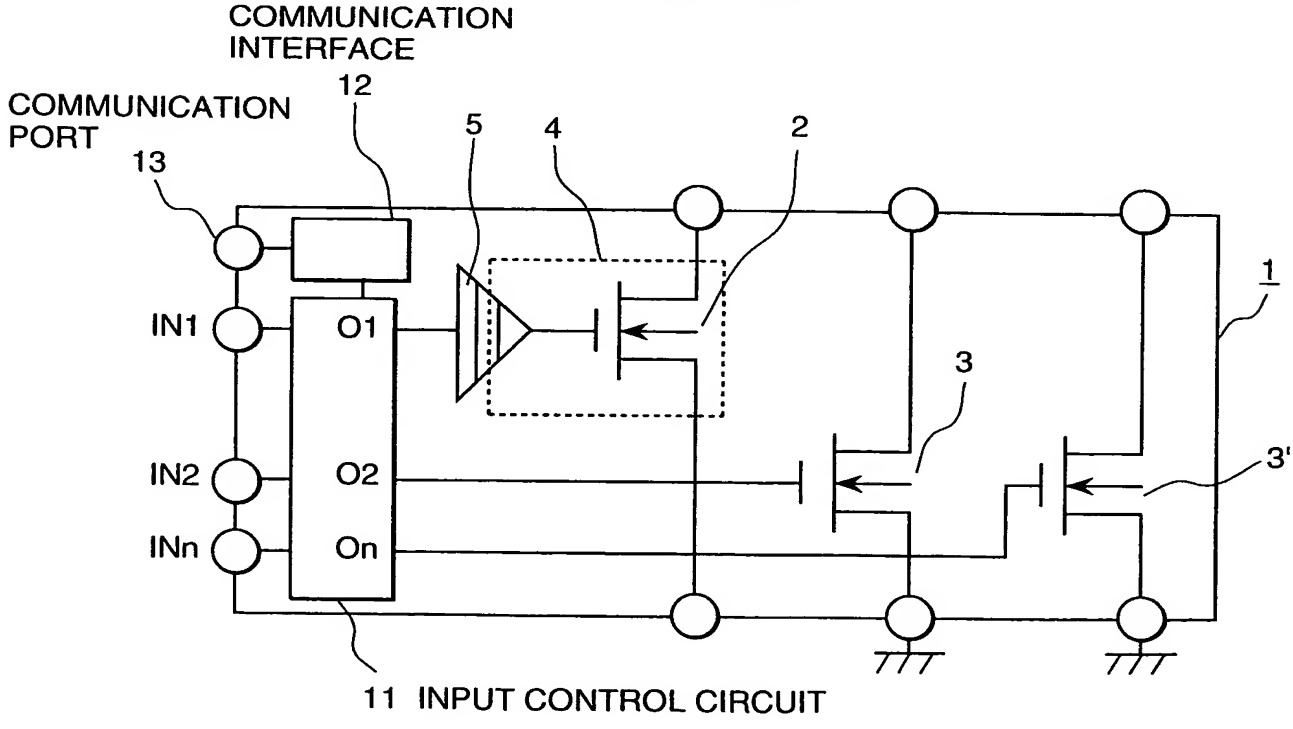

COMMUNICATION INTERFACE
12
COMMUNICATION PORT
13
5
4
2
1
IN1
O1
3
IN2
O2
3'
INn
On
11 INPUT CONTROL CIRCUIT

FIG. 16

IN1	IN2	O1	O2
L	L	L	L
L	H	L	H
H	L	H	L
H	H	L	L

FIG. 17

IN1	O1	O2
L	L	L
H	H	H

FIG. 18

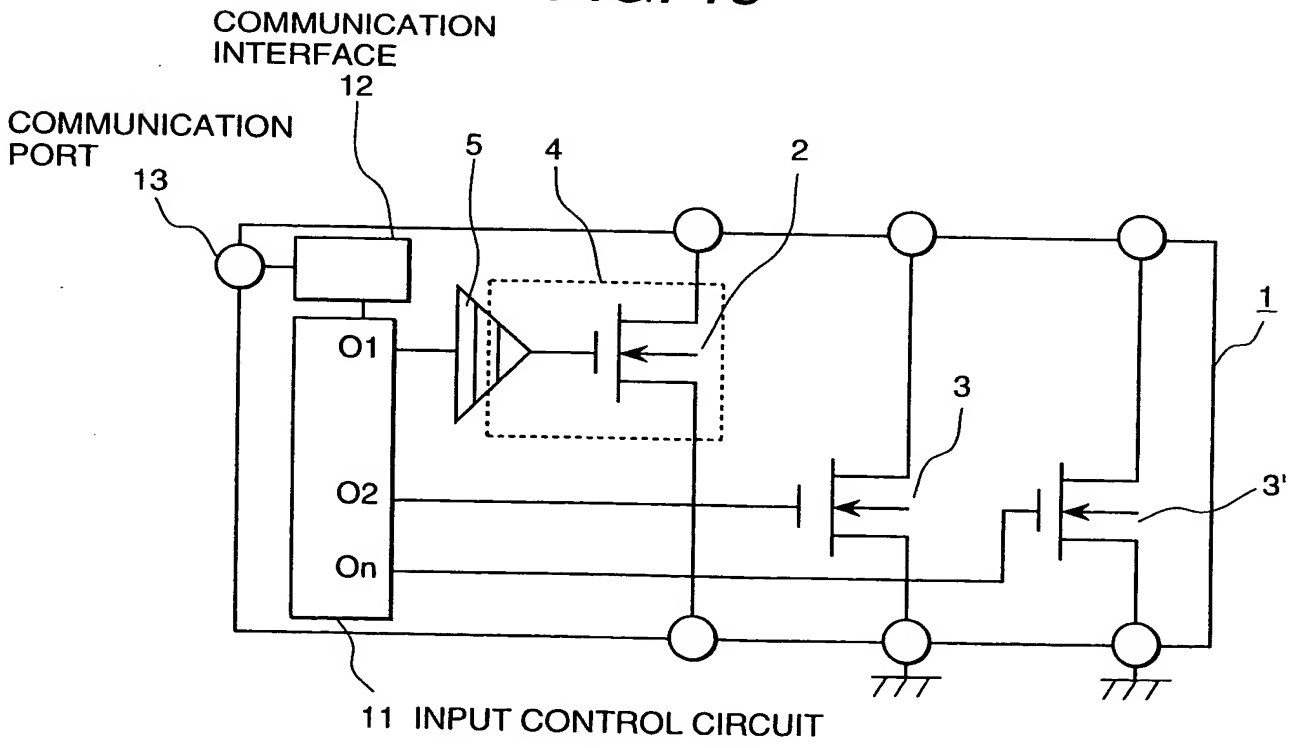


FIG. 19

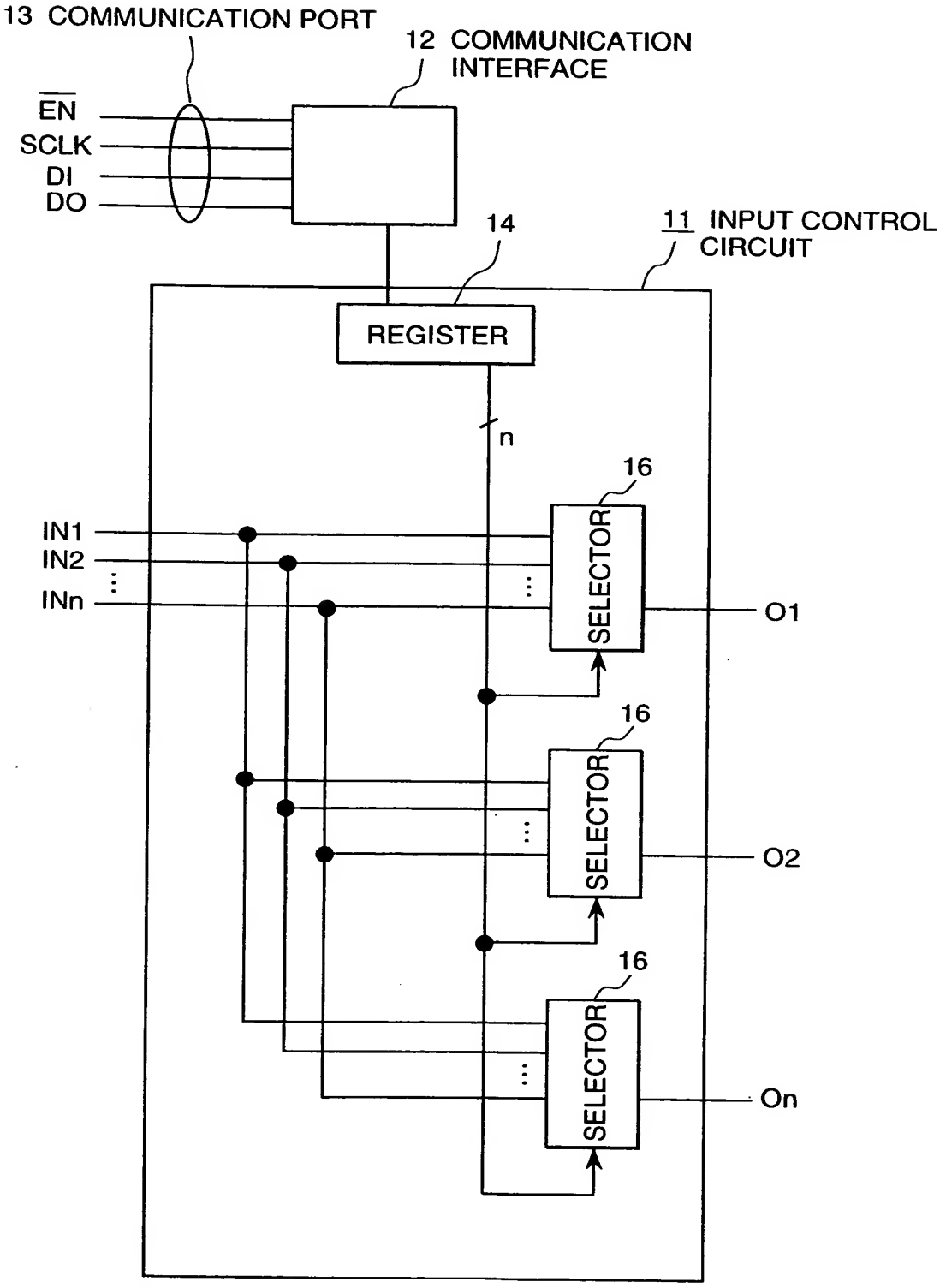

13 COMMUNICATION PORT
12 COMMUNICATION INTERFACE
EN
SCLK
DI
DO
14
11 INPUT CONTROL CIRCUIT
REGISTER
n
16
IN1
IN2
INn
SELECTOR
O1
16
SELECTOR
O2
16
SELECTOR
On

FIG. 20

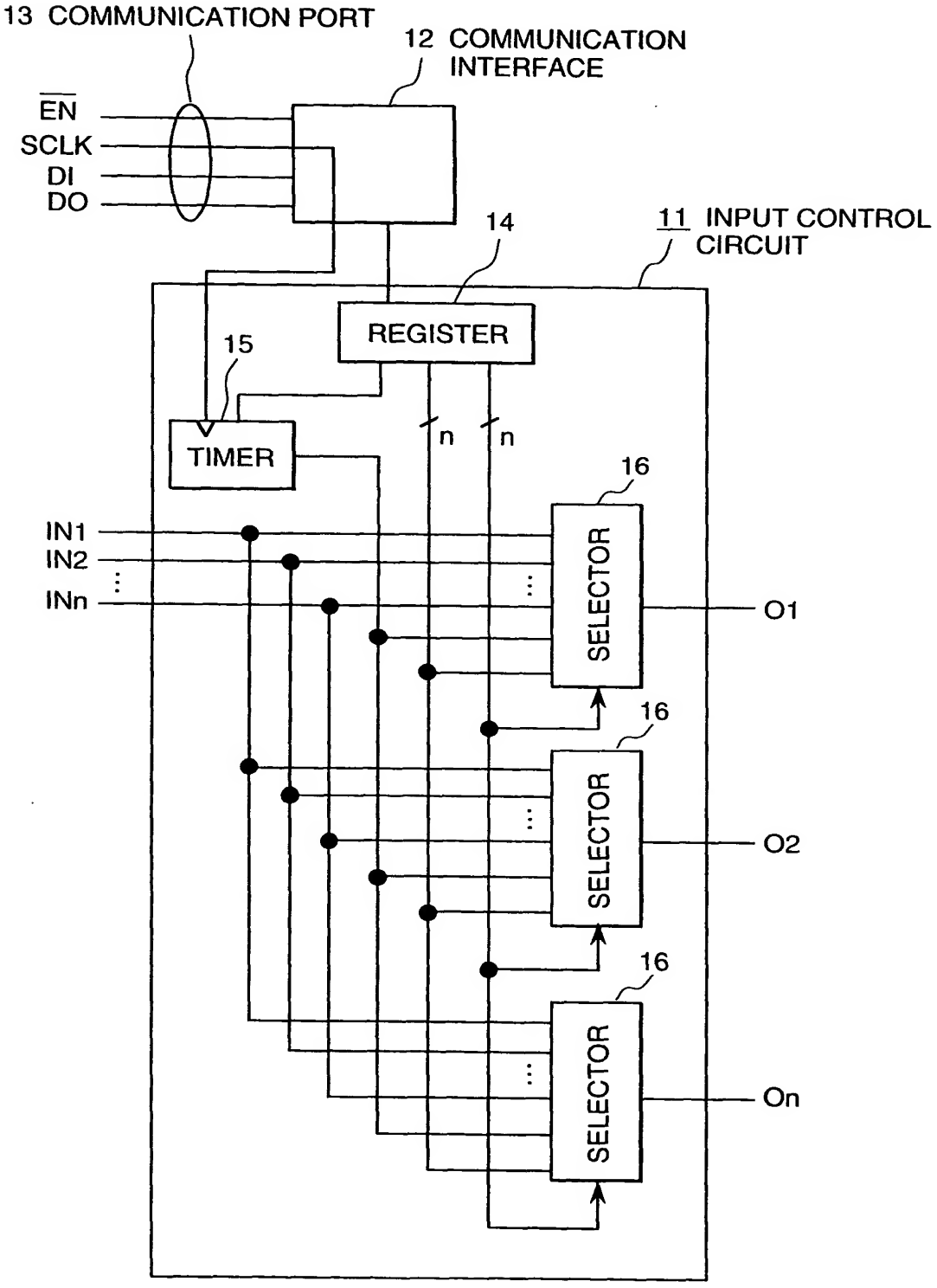

13 COMMUNICATION PORT
12 COMMUNICATION INTERFACE
EN
SCLK
DI
DO
14
11 INPUT CONTROL CIRCUIT
REGISTER
15
TIMER
n
n
16
IN1
IN2
INn
SELECTOR
O1
16
SELECTOR
O2
16
SELECTOR
On

FIG. 21

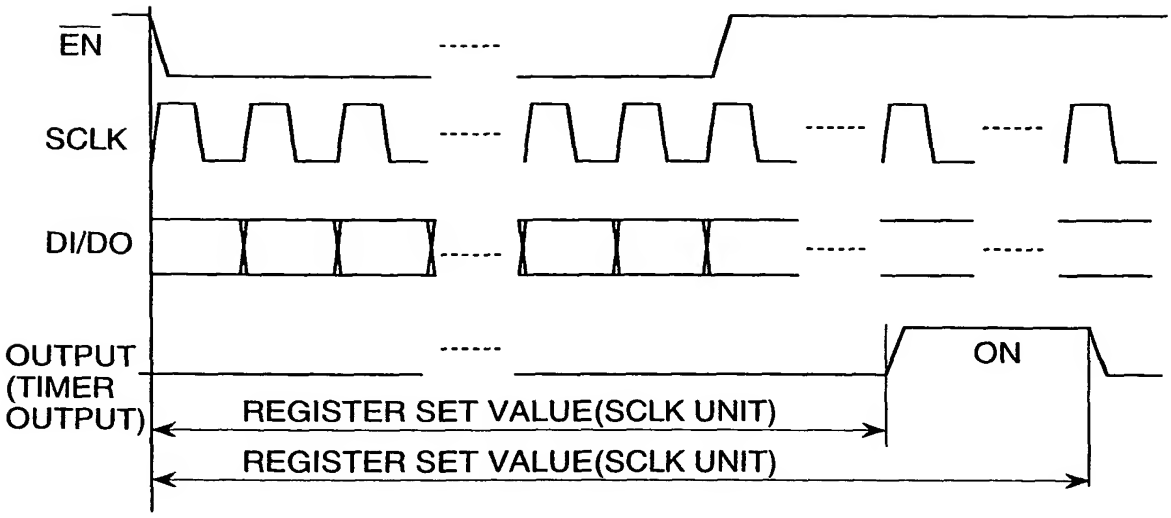

EN
SCLK
DI/DO
OUTPUT
(TIMER
OUTPUT)
ON
REGISTER SET VALUE(SCLK UNIT)
REGISTER SET VALUE(SCLK UNIT)

FIG. 22

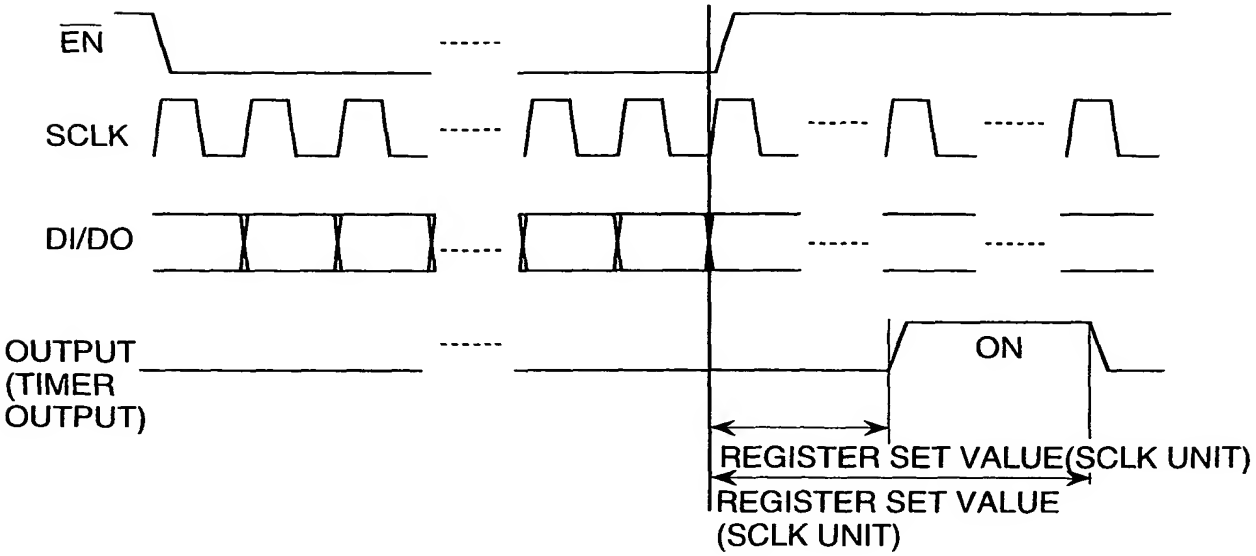

EN
SCLK
DI/DO
OUTPUT
(TIMER
OUTPUT)
ON
REGISTER SET VALUE(SCLK UNIT)
REGISTER SET VALUE
(SCLK UNIT)

FIG. 23

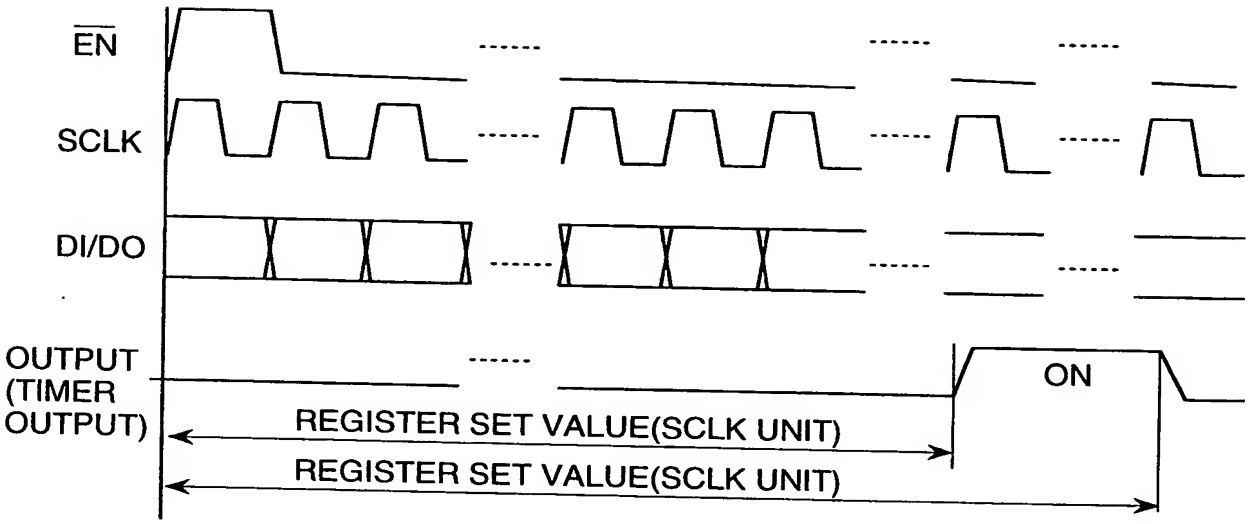

EN
SCLK
DI/DO
OUTPUT
(TIMER
OUTPUT)
ON
REGISTER SET VALUE(SCLK UNIT)
REGISTER SET VALUE(SCLK UNIT)

FIG. 24

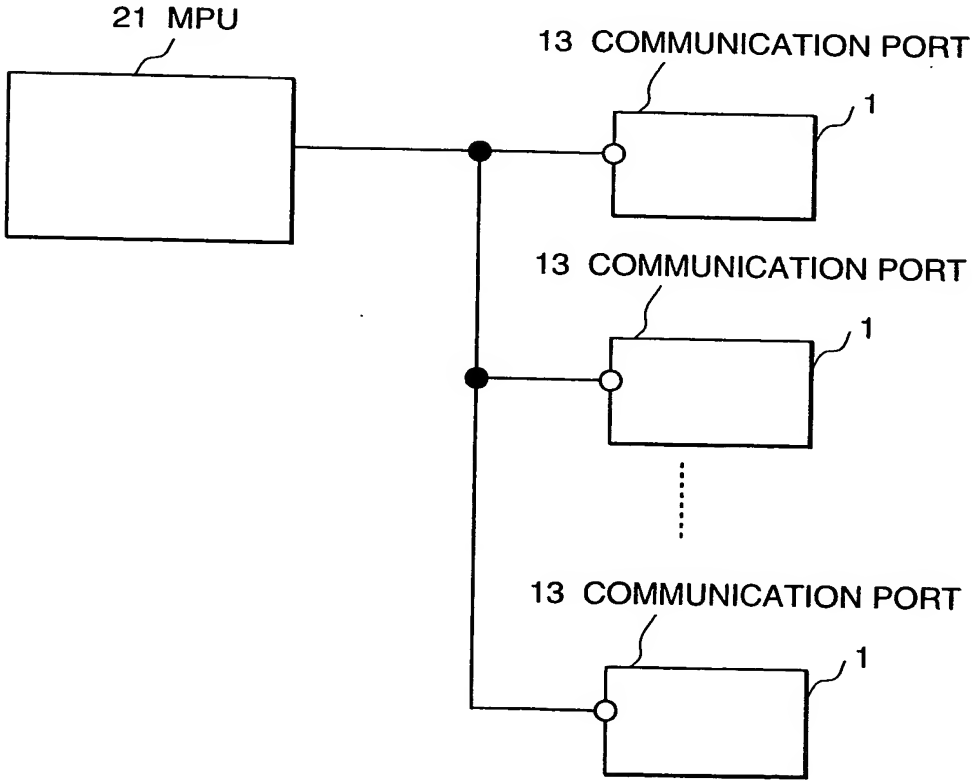

21 MPU
13 COMMUNICATION PORT
1
13 COMMUNICATION PORT
1
13 COMMUNICATION PORT
1

FIG. 25

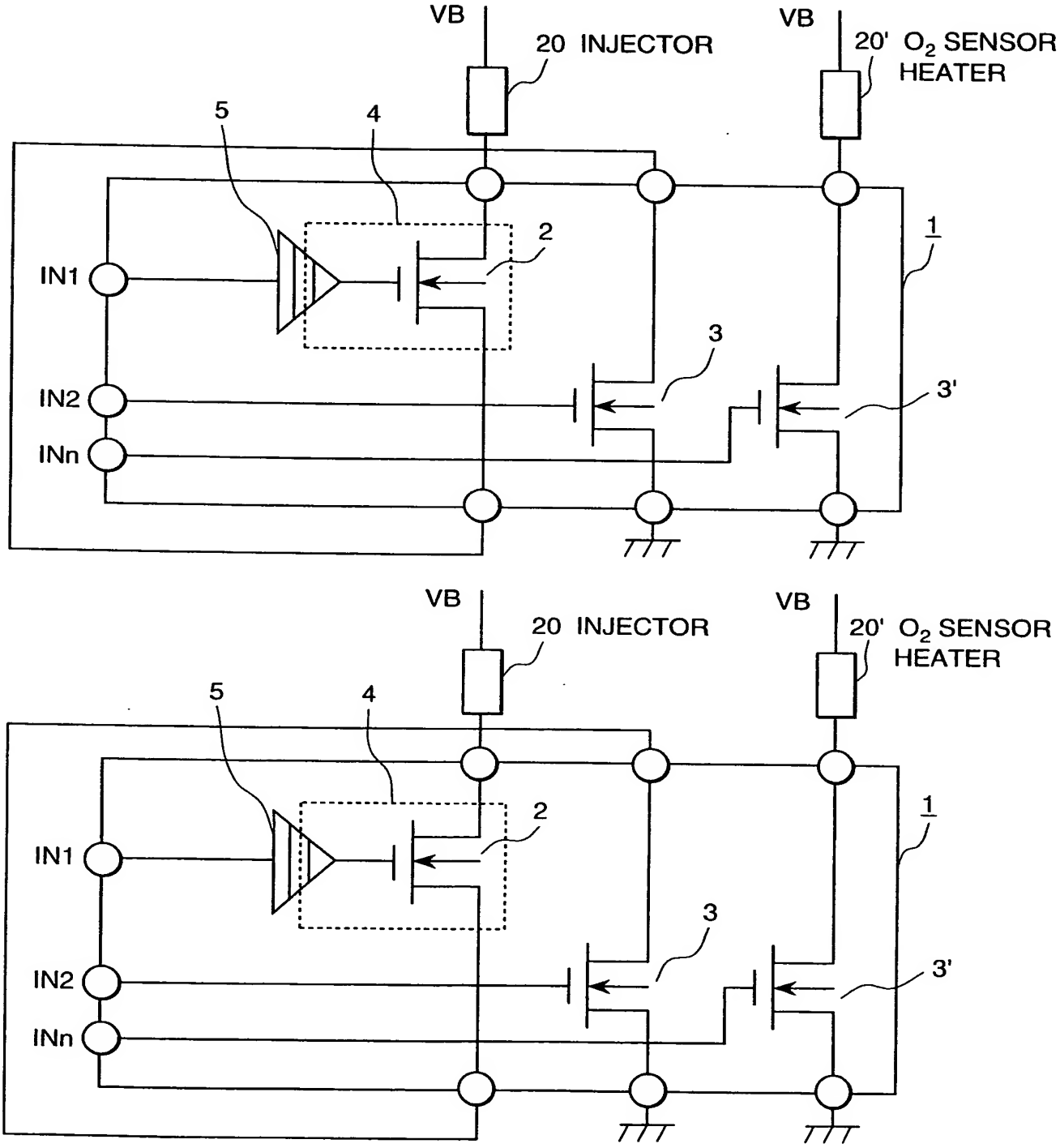

VB
20 INJECTOR
VB
20' O_2 SENSOR HEATER
5
4
2
1
IN1
3
IN2
3'
INn
VB
20 INJECTOR
VB
20' O_2 SENSOR HEATER
5
4
2
1
IN1
3
IN2
3'
INn

FIG. 26

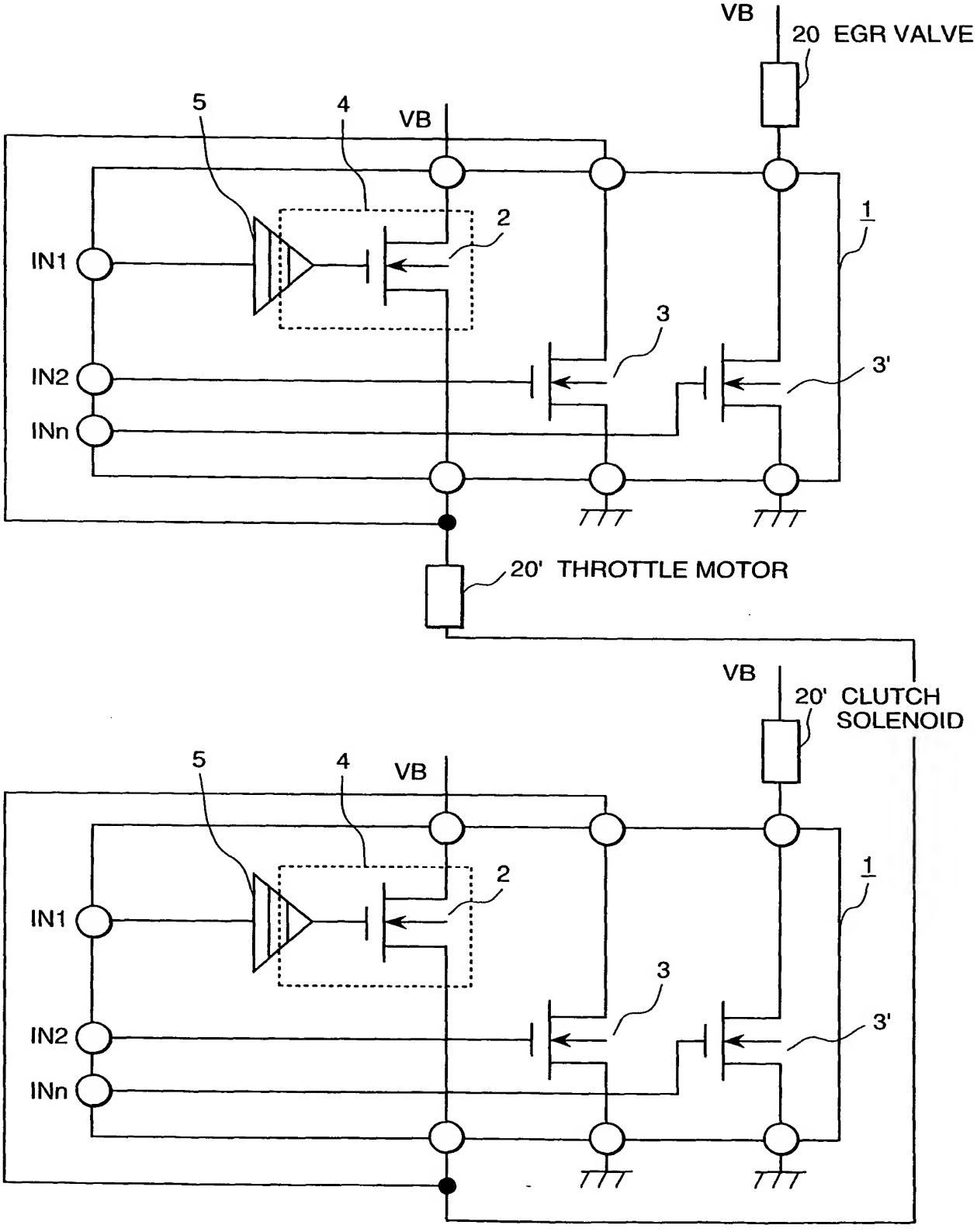

VB
20 EGR VALVE
5
4
VB
2
1
IN1
3
IN2
3'
INn
20' THROTTLE MOTOR
VB
20' CLUTCH SOLENOID
5
4
VB
2
1
IN1
3
IN2
3'
INn

FIG. 27

LSI	CHANNEL	WITHSTAND VOLTAGE		ON RESISTANCE		USE		
						FOR 4 CYLINDERS	FOR 6 CYLINDERS	FOR 8 CYLINDERS
1	1a	40V	80V	0.3Ω	0.6Ω	INJECTOR 1	INJECTOR 1	INJECTOR 1
	1b	40V		0.3Ω				
	2a	40V	80V	0.3Ω	0.6Ω	INJECTOR 2	INJECTOR 2	INJECTOR 2
	2b	40V		0.3Ω				
	3a	40V	80V	0.3Ω	0.6Ω	INJECTOR 3	INJECTOR 3	INJECTOR 3
	3b	40V		0.3Ω				
	4a	40V	80V	0.3Ω	0.6Ω	INJECTOR 4	INJECTOR 4	INJECTOR 4
	4b	40V		0.3Ω				
	5a	40V	80V	0.3Ω	0.6Ω	LOW PRES. LOAD	INJECTOR 5	LOW PRES. LOAD
	5b	40V		0.3Ω		LOW PRES. LOAD		LOW PRES. LOAD
	6a	40V	80V	0.3Ω	0.6Ω	LOW PRES. LOAD	INJECTOR 6	LOW PRES. LOAD
	6b	40V		0.3Ω		LOW PRES. LOAD		LOW PRES. LOAD
	7～n	40V		0.3Ω		LOW PRES. LOAD	LOW PRES. LOAD	LOW PRES. LOAD
2	1a	40V	80V	0.3Ω	0.6Ω			INJECTOR 5
	1b	40V		0.3Ω				
	2a	40V	80V	0.3Ω	0.6Ω			INJECTOR 6
	2b	40V		0.3Ω				
	3a	40V	80V	0.3Ω	0.6Ω			INJECTOR 7
	3b	40V		0.3Ω				
	4a	40V	80V	0.3Ω	0.6Ω			INJECTOR 8
	4b	40V		0.3Ω				
	5a	40V	80V	0.3Ω	0.6Ω			LOW PRES. LOAD
	5b	40V		0.3Ω				LOW PRES. LOAD
	6a	40V	80V	0.3Ω	0.6Ω			LOW PRES. LOAD
	6b	40V		0.3Ω				LOW PRES. LOAD
	7～n	40V		0.3Ω				LOW PRES. LOAD

FIG. 28

LSI	CHAN-NEL	WITHSTAND VOLTAGE		ON RESISTANCE		USE		
						FOR 4 CYLINDERS	FOR 6 CYLINDERS	FOR 8 CYLINDERS
1	1	80V		0.6Ω		INJECTOR 1	INJECTOR 1	INJECTOR 1
	2	80V		0.6Ω		INJECTOR 2	INJECTOR 2	INJECTOR 2
	3	80V		0.6Ω		INJECTOR 3	INJECTOR 3	INJECTOR 3
	4	80V		0.6Ω		INJECTOR 4	INJECTOR 4	INJECTOR 4
	5a	40V	80V	0.3Ω	0.6Ω	LOW PRES. LOAD	INJECTOR 5	LOW PRES. LOAD
	5b	40V		0.3Ω		LOW PRES. LOAD		LOW PRES. LOAD
	6a	40V	80V	0.3Ω	0.6Ω	LOW PRES. LOAD	INJECTOR 6	LOW PRES. LOAD
	6b	40V		0.3Ω		LOW PRES. LOAD		LOW PRES. LOAD
	7～n	40V		0.3Ω		LOW PRES. LOAD	LOW PRES. LOAD	LOW PRES. LOAD
2	1	80V		0.6Ω				INJECTOR 5
	2	80V		0.6Ω				INJECTOR 6
	3	80V		0.6Ω				INJECTOR 7
	4	80V		0.6Ω				INJECTOR 8
	5a	40V	80V	0.3Ω	0.6Ω			LOW PRES. LOAD
	5b	40V		0.3Ω				LOW PRES. LOAD
	6a	40V	80V	0.3Ω	0.6Ω			LOW PRES. LOAD
	6b	40V		0.3Ω				LOW PRES. LOAD
	7～n	40V		0.3Ω				LOW PRES. LOAD

FIG. 29

LSI	CHANNEL	WITHSTAND VOLTAGE		USE		
				FOR 4 CYLINDERS	FOR 6 CYLINDERS	FOR 8 CYLINDERS
1	1	400V		IGNITER 1	IGNITER 1	IGNITER 1
	2	400V		IGNITER 2	IGNITER 2	IGNITER 2
	3	400V		IGNITER 3	IGNITER 3	IGNITER 3
	4	400V		IGNITER 4	IGNITER 4	IGNITER 4
	5a	40V	400V	LOW PRES. LOAD	IGNITER 5	LOW PRES. LOAD
	5j	40V		LOW PRES. LOAD		LOW PRES. LOAD
	6a	40V	400V	LOW PRES. LOAD	IGNITER 6	LOW PRES. LOAD
	6j	40V		LOW PRES. LOAD		LOW PRES. LOAD
	7～n	40V		LOW PRES. LOAD	LOW PRES. LOAD	LOW PRES. LOAD
2	1	400V				IGNITER 5
	2	400V				IGNITER 6
	3	400V				IGNITER 7
	4	400V				IGNITER 8
	5a	40V	400V			LOW PRES. LOAD
	5j	40V				LOW PRES. LOAD
	6a	40V	400V			LOW PRES. LOAD
	6j	40V				LOW PRES. LOAD
	7～n	40V				LOW PRES. LOAD

FIG. 30

LSI	CHANNEL	WITHSTAND VOLTAGE		ON RESISTANCE		USE		
						14 (12) V SYSTEM	42V SYSTEM	MIXED BOTH SYSTEMS
1	1a	40V	80V	0.3Ω	0.6Ω	14 (12) V SYSTEM LOAD	42V SYSTEM LOAD	42V SYSTEM LOAD
	1b	40V		0.3Ω		14 (12) V SYSTEM LOAD		
	2a	40V	80V	0.3Ω	0.6Ω	14 (12) V SYSTEM LOAD	42V SYSTEM LOAD	42V SYSTEM LOAD
	2b	40V		0.3Ω		14 (12) V SYSTEM LOAD		
	3a	40V	80V	0.3Ω	0.6Ω	14 (12) V SYSTEM LOAD	42V SYSTEM LOAD	42V SYSTEM LOAD
	3b	40V		0.3Ω		14 (12) V SYSTEM LOAD		
	4a	40V	80V	0.3Ω	0.6Ω	14 (12) V SYSTEM LOAD	42V SYSTEM LOAD	42V SYSTEM LOAD
	4b	40V		0.3Ω		14 (12) V SYSTEM LOAD		
	⋮							
	na	40V	80V	0.3Ω	0.6Ω	14 (12) V SYSTEM LOAD	42V SYSTEM LOAD	14 (12) V SYSTEM LOAD
	nb	40V		0.3Ω		14 (12) V SYSTEM LOAD		14 (12) V SYSTEM LOAD

FIG. 31

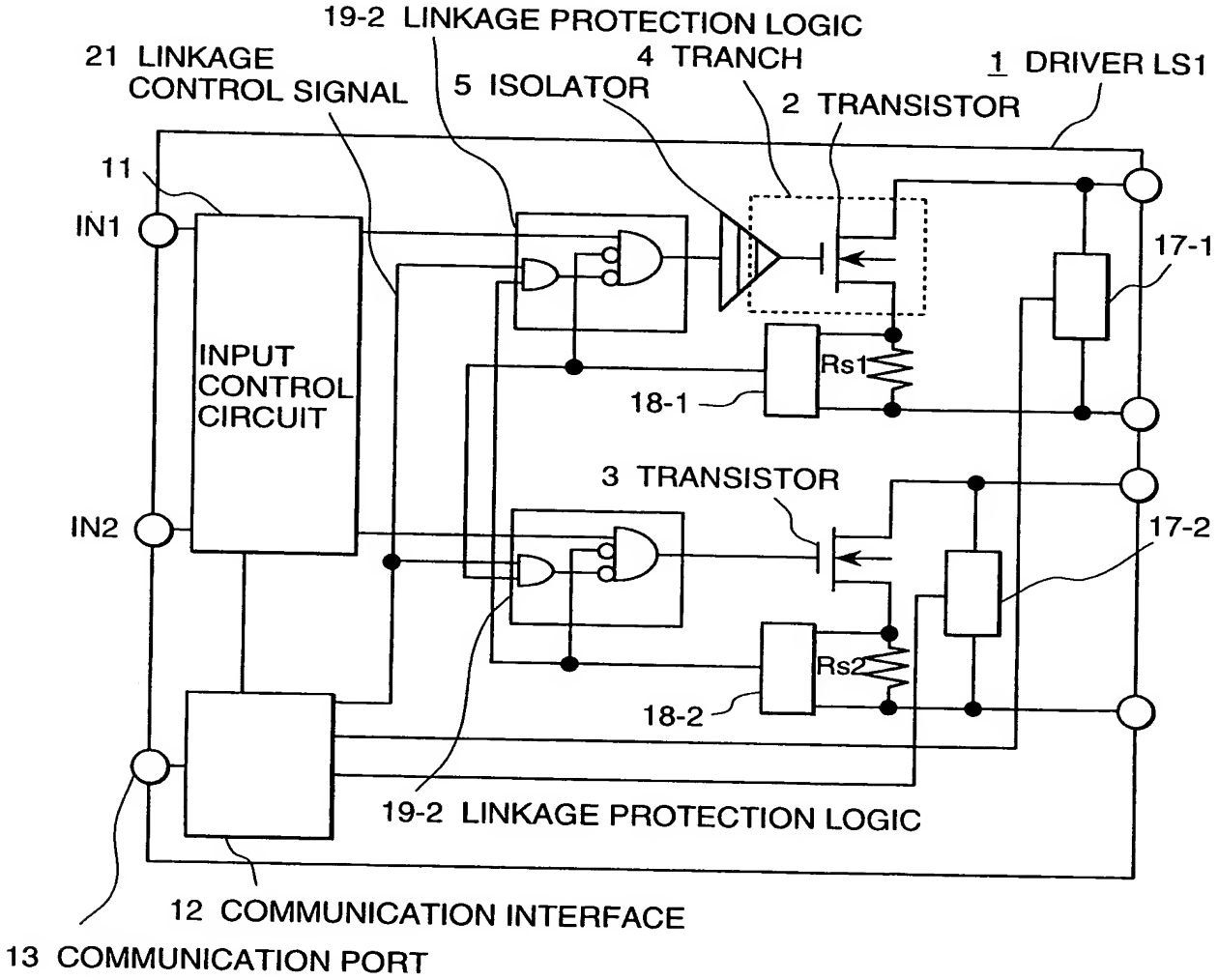

19-2 LINKAGE PROTECTION LOGIC
21 LINKAGE CONTROL SIGNAL
4 TRANCH
5 ISOLATOR
2 TRANSISTOR
1 DRIVER LS1
11
IN1
17-1
INPUT CONTROL CIRCUIT
Rs1
18-1
3 TRANSISTOR
IN2
17-2
Rs2
18-2
19-2 LINKAGE PROTECTION LOGIC
12 COMMUNICATION INTERFACE
13 COMMUNICATION PORT

FIG. 32

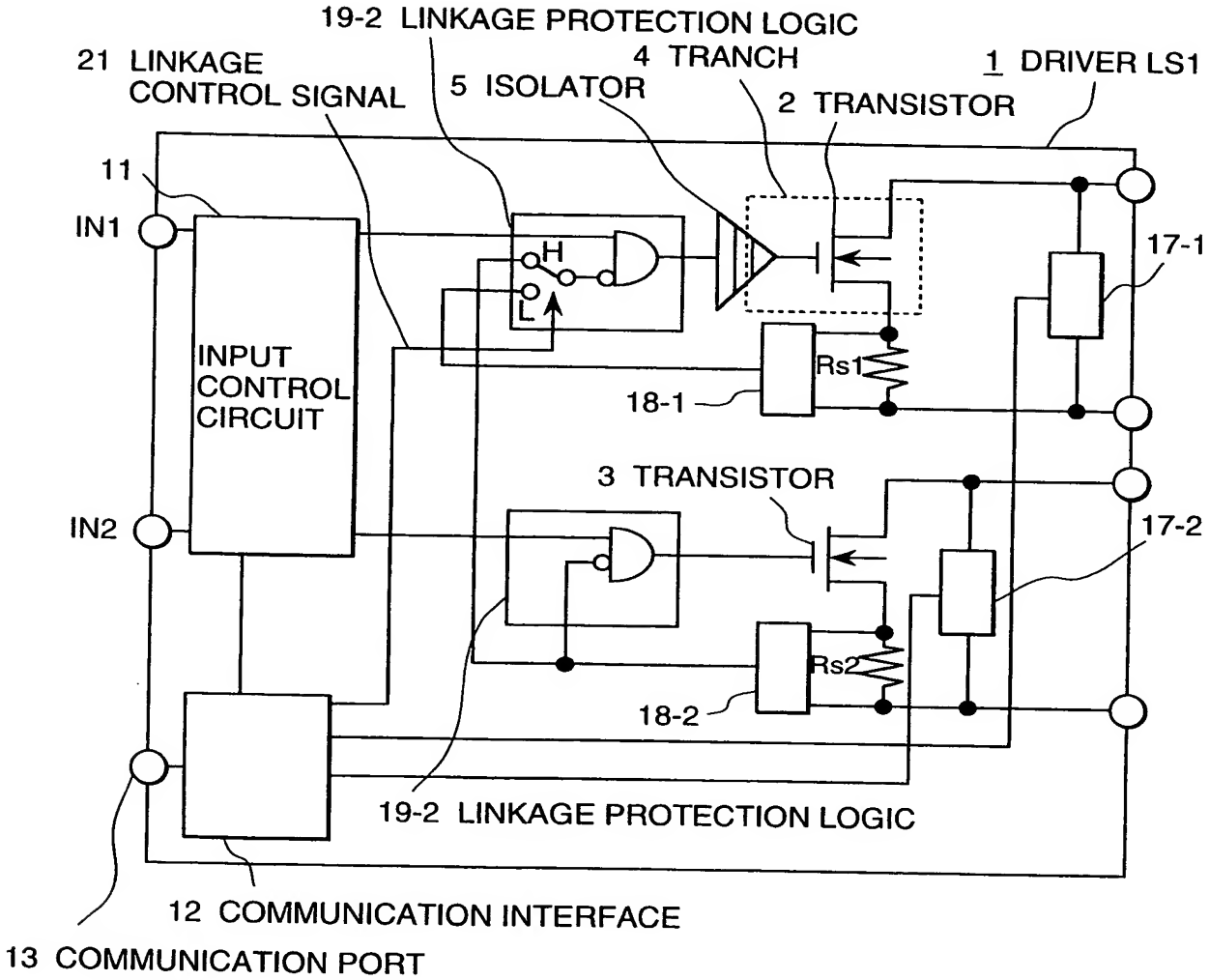
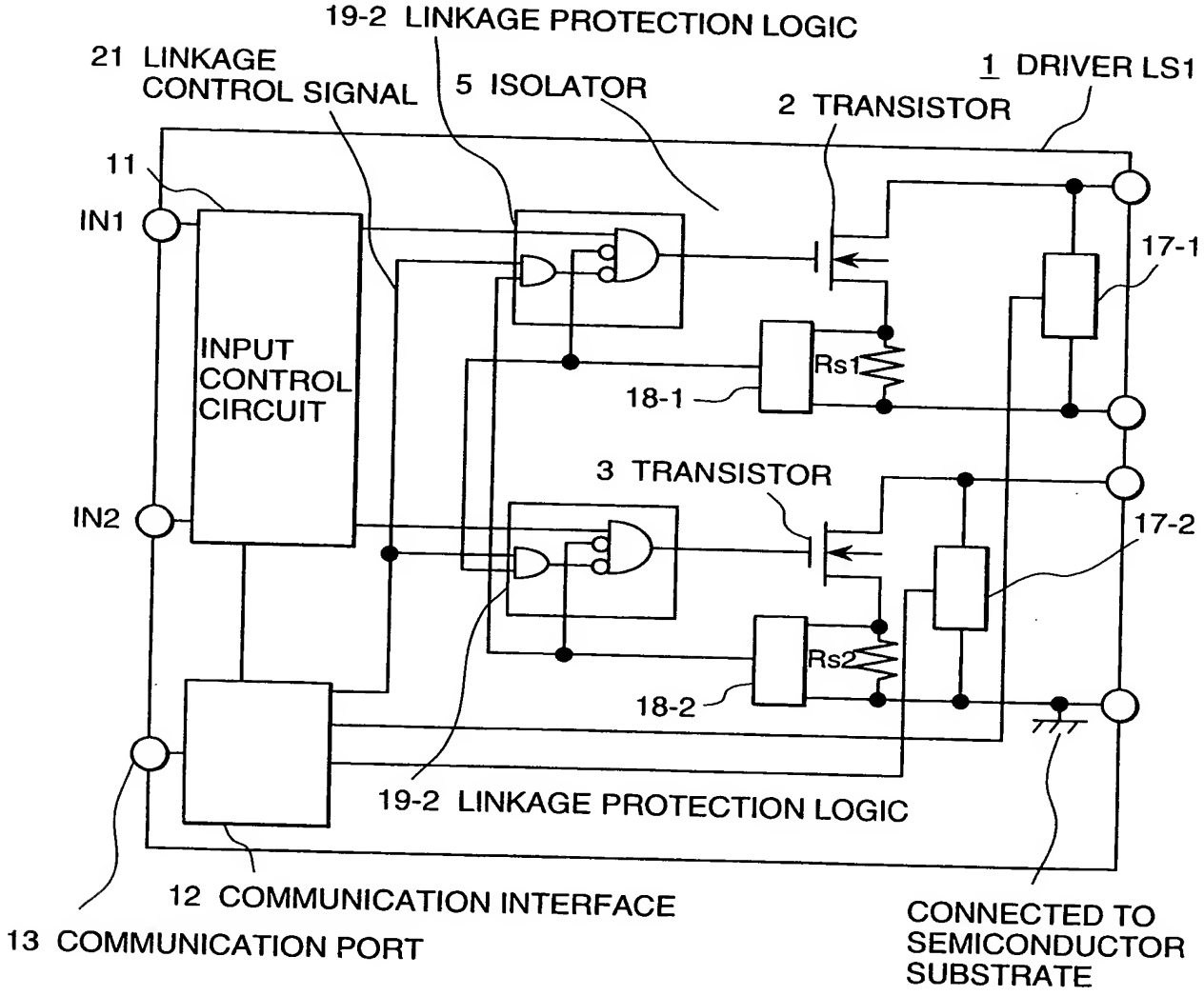

19-2 LINKAGE PROTECTION LOGIC
21 LINKAGE CONTROL SIGNAL
4 TRANCH
5 ISOLATOR
2 TRANSISTOR
1 DRIVER LS1
11
IN1
H
L
17-1
INPUT CONTROL CIRCUIT
Rs1
18-1
3 TRANSISTOR
IN2
17-2
Rs2
18-2
19-2 LINKAGE PROTECTION LOGIC
12 COMMUNICATION INTERFACE
13 COMMUNICATION PORT

FIG. 33


19-2 LINKAGE PROTECTION LOGIC
21 LINKAGE CONTROL SIGNAL
5 ISOLATOR
1 DRIVER LS1
2 TRANSISTOR
11
IN1
17-1
INPUT CONTROL CIRCUIT
Rs1
18-1
3 TRANSISTOR
IN2
17-2
Rs2
18-2
19-2 LINKAGE PROTECTION LOGIC
12 COMMUNICATION INTERFACE
13 COMMUNICATION PORT
CONNECTED TO SEMICONDUCTOR SUBSTRATE